FORM PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO. 10001121-1	SERIAL NO. 00/000,000
	APPLICANT K nneth P. Park r	
	FILING DATE Unknown	GROUP Unk

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS
	1A					
	1B					
	1C					
	1D					
	1E					
	1F					
	1G					
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	1I					
	1J					
	1K					

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	TRANSLATION YES	TRANSLATION NO
	1L							
	1M							
	1N							
	1O							
	1P							

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

ED	1Q	"A Logic Design Structure for LSI Testability", E.B. Eichelberger and T.W. Williams, Proc. 14th Design Automation Conf. IEEE Pub. 77CH1216-1C, June 1977, pp 462-468
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EXAMINER	DATE CONSIDERED
[signature]	08/22/06

FORM PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO. 10001121-1	SERIAL NO. 00/000,000
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	FILING DATE Unknown	GROUP Unk

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS
	2A					
	2B					
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	2K					

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	TRANSLATION YES	TRANSLATION NO
	2L							
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EP	2Q	"Design for Testability - A Survey", T.W. Williams and K.P. Parker, Proceedings of the IEEE, Jan. 1983, Vol 71, no. 1, pp 98-112
EP	2R	"The Boundary Scan Cell", Texas Instruments, JTAG IEEE 1149.1/P1149.4 Tutorial, Sept. 1997, Tut.I-20, Tut II-24-26
EP	2S	

EXAMINER	DATE CONSIDERED
Shu A	08/22/06

Rev 5/01 (PTO1449)